Abstract of the Disclosure

Formation of elements of a vertical transistor is described, particularly, a gate-source-drain arrangement of a CMOS transistor. Vertical transistors are used frequently in the integrated circuit art. Accordingly, improved methods for their formation, which are not limited by constraints of photolithography, have great utility and importance. Those of skill in the art will appreciate that the techniques described may be used to fabricate other types of devices as well. For example, junctions of a bipolar transistor (as well as other device junction types) may be fabricated using the methods described herein.